Bare Die fcPoP

Flip Chip Package-on-Package: fcVFBGA-PoPb, fcWFBGA-PoPb

Specifications (fcPoP)

Die Thickness	Minimum 60mm
FC Bump Pitch	Minimum 140mm (Pb-free) Minimum 80mm/40mm (Cu/SnAg)
FC Bumps*	Pb-free, Cu pillar
Solder Balls	Sn/Ag/Cu (Pb-free ball)
Marking	Laser
Packing Options	JEDEC tray or tape & reel

*Refer to fcCuBE datasheet for PoP package details using Cu pillar interconnect.

Reliability

Moisture Sensitivity Level	JEDEC Level 2A, (60% RH/60°C), 120 hrs
Temperature Cycling	Condition B (-55°C/+125°C, 1000 cycles)
Temp/Humidity Cycling	85°C/85% RH, 1000 hrs
Highly Accelerated Stress Test	135°C/85% RH, 96 hrs
High Temperature Storage	150°C, 1000 hrs

Thermal Performance

Thermal behavior is determined by the exact configuration of the overall structure and the distribution of power dissipation among all of the die. During the package design process, we provide quick-turn thermal feasibility analysis and data as needed to help ensure proper thermal operation.

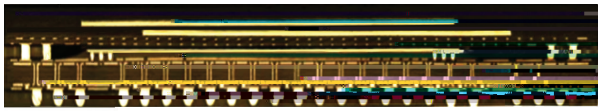
Package	Leads	Die Size (mm)	Power (W)	T_A (°C)	Airflow (m/s)	T_J (°C)	θja (°C/W)
12 x 12mm fcPoP	753	7 x 7 x 0.1	2	25.0	NC**	71.9	23.4
14 x 14mm fcPoP	641	8 x 8 x 0.1	2	25.0	NC**	70.0	22.5
15 x 15mm fcPoP	992	8.6 x 10.9 x 0.1					

Notes: *Typical bottom fcPoP thermal performance. Data for bottom PoP only without the effect of top PoP package. Substrate 4 layer laminate build-up (1/2/1). Simulation data for package mounted on 4 layer PCB per JEDEC JES51-9 under natural convection. **NC=Natural Convection

Electrical Performance

The electrical behavior is highly dependent on the package layout and the substrate structures. 3D electrical simulation is used to predict the actual electrical behavior once designs are partially or fully completed. As expected, the electrical performance advantage of using flip chip over wire bond is seen in these packages.

Cross Sections



Package	Wire Bond	Flip Chip Interconnect	Body Size (mm)	BGA Pitch (mm)	Top Pitch (mm)
Bare Die PoP	No	Pb-free	10x10 ~ 15x15	min 0.4	0.5
		Cu/Sn/Ag			0.4